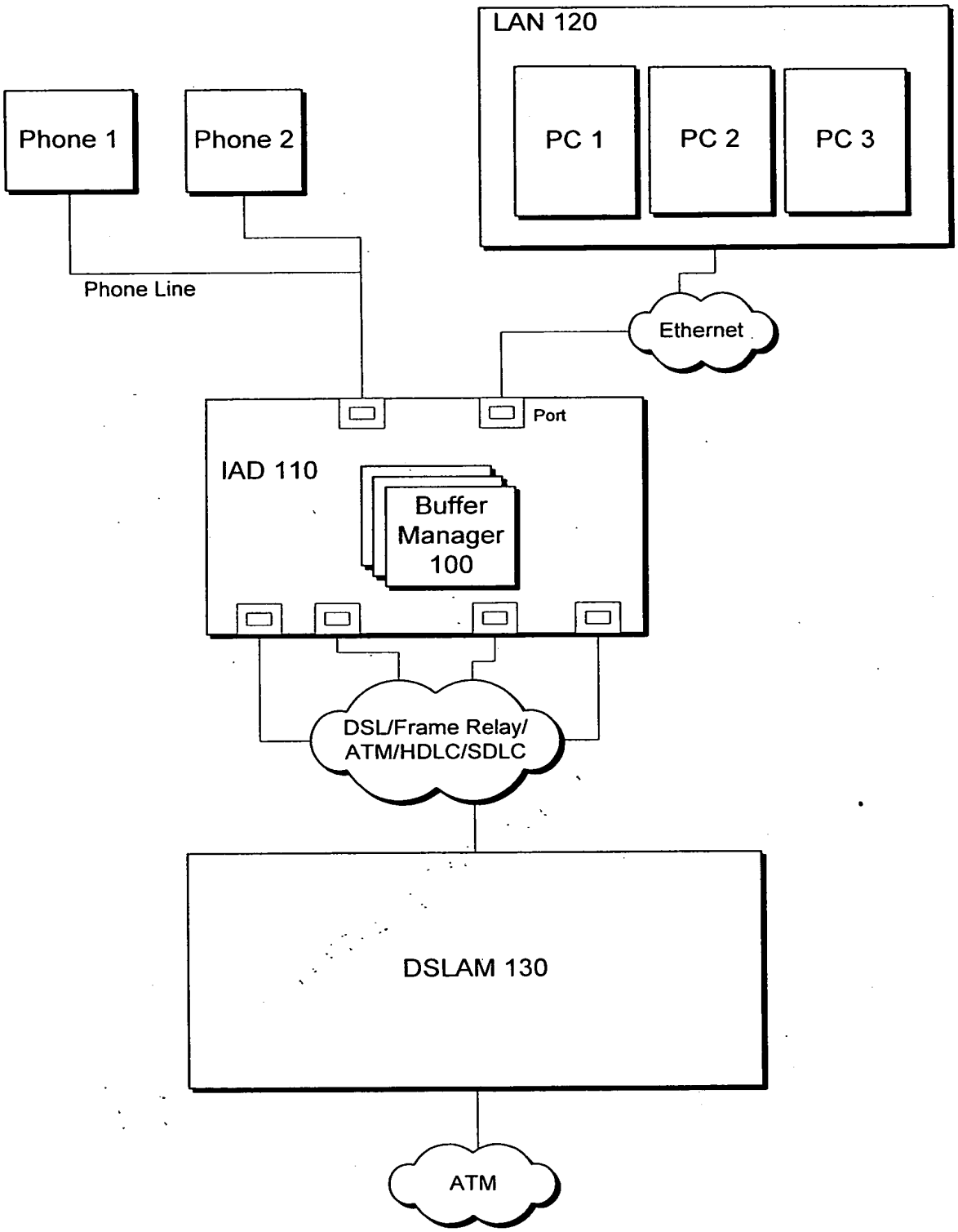

LAN 120
PC 1
PC 2
PC 3
Phone 1
Phone 2
Phone Line
Ethernet
Port
IAD 110
Buffer Manager 100
DSL/Frame Relay/ ATM/HDLC/SDLC
DSLAM 130
ATM

FIG. 1

Patent Application

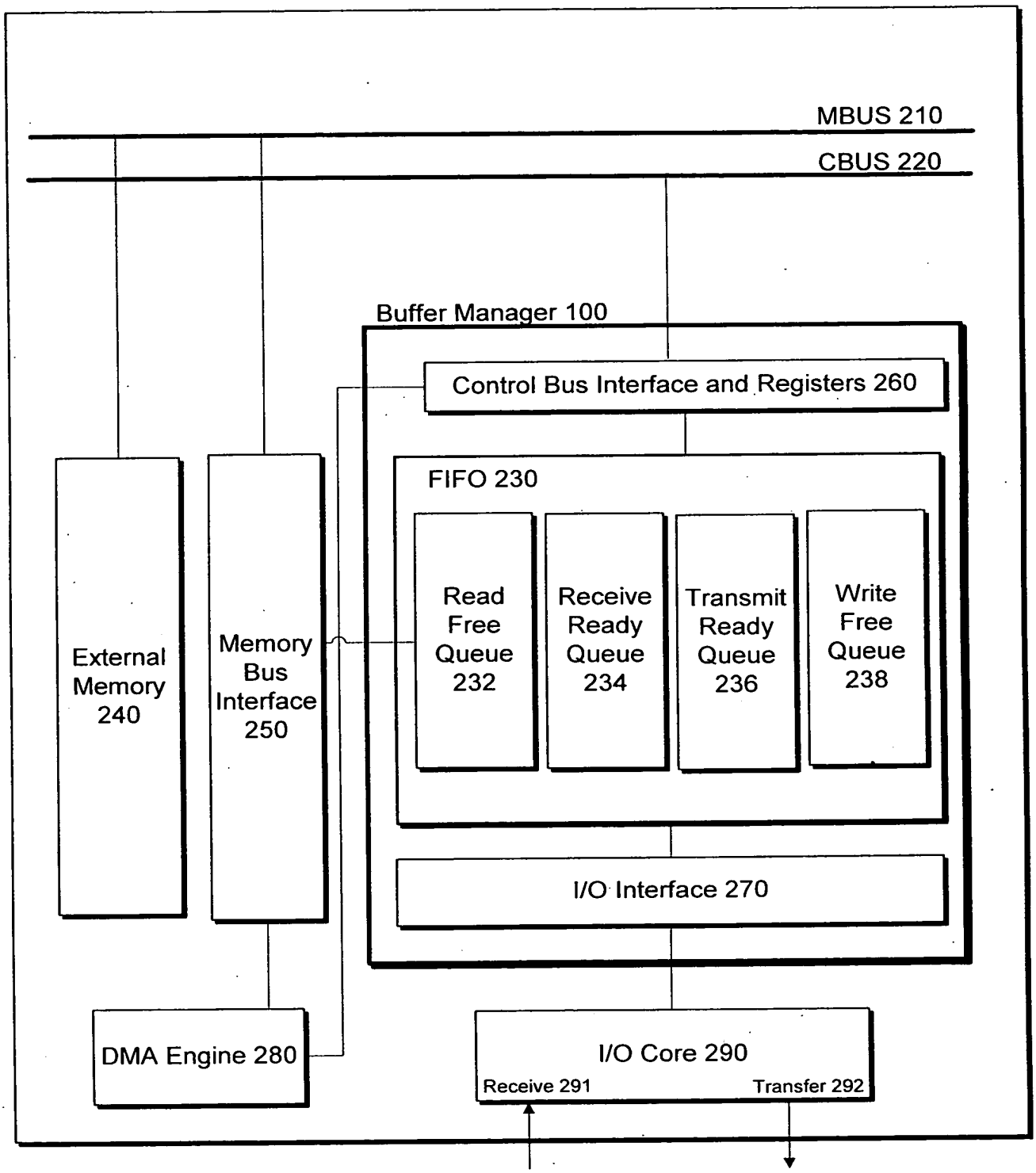


FIG. 2

10/24/2003, EAST Version: 1.04.0000

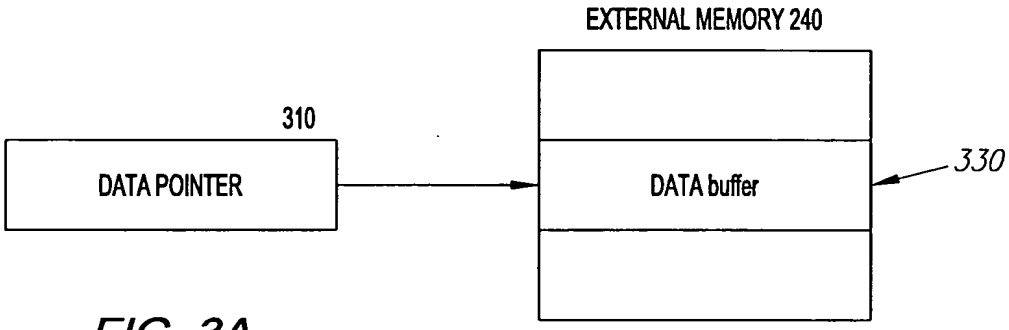


FIG. 3A

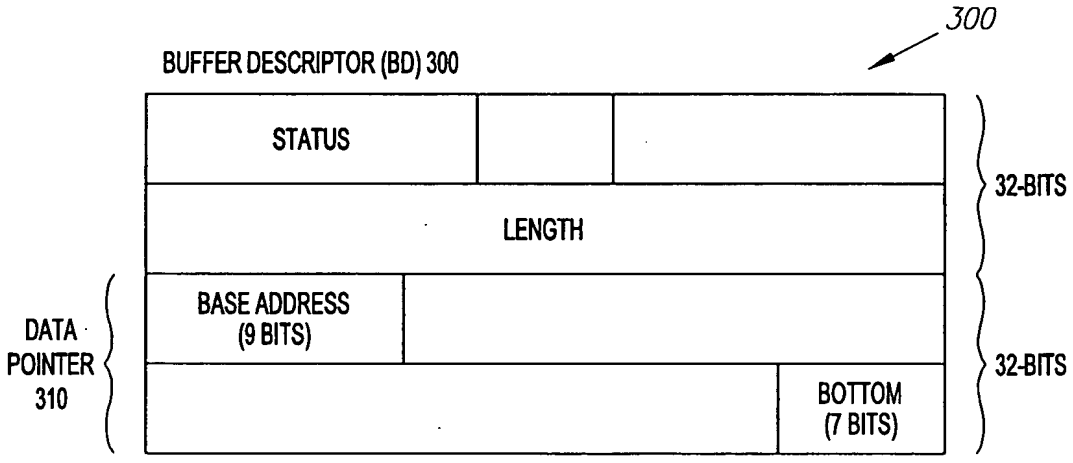
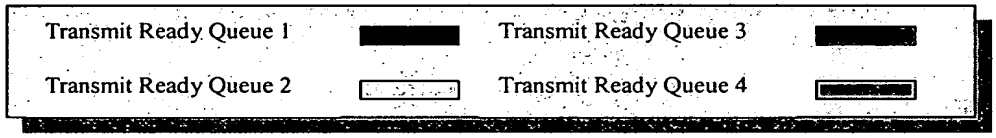


FIG. 3B

Configuration	Bit 8	Bit 7	Transmit Queue #	Depth
1	0	0	1-4	32
2	0	1	1-2	40
			3-4	24
3	1	0	1	80
			2-3	24
			4	0
4	1	1	1	64
			2	64
			3	0
			4	0

Transmit Ready Queue Configuration



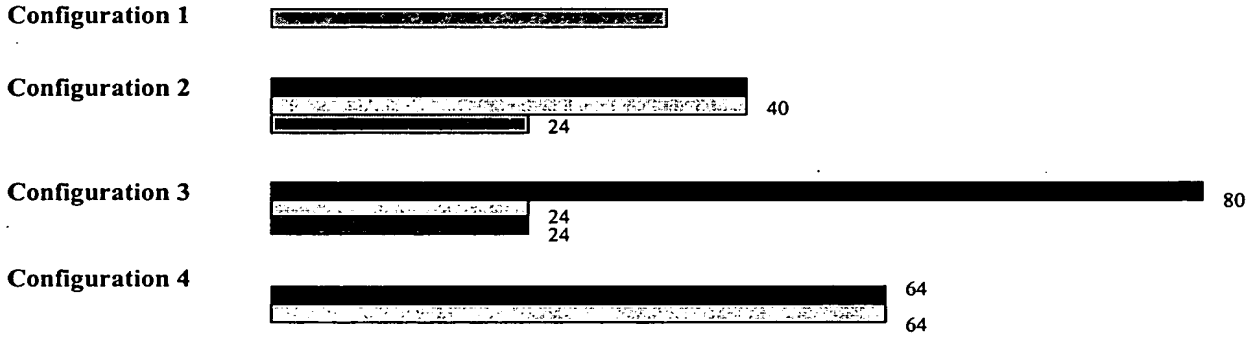


FIG. 4

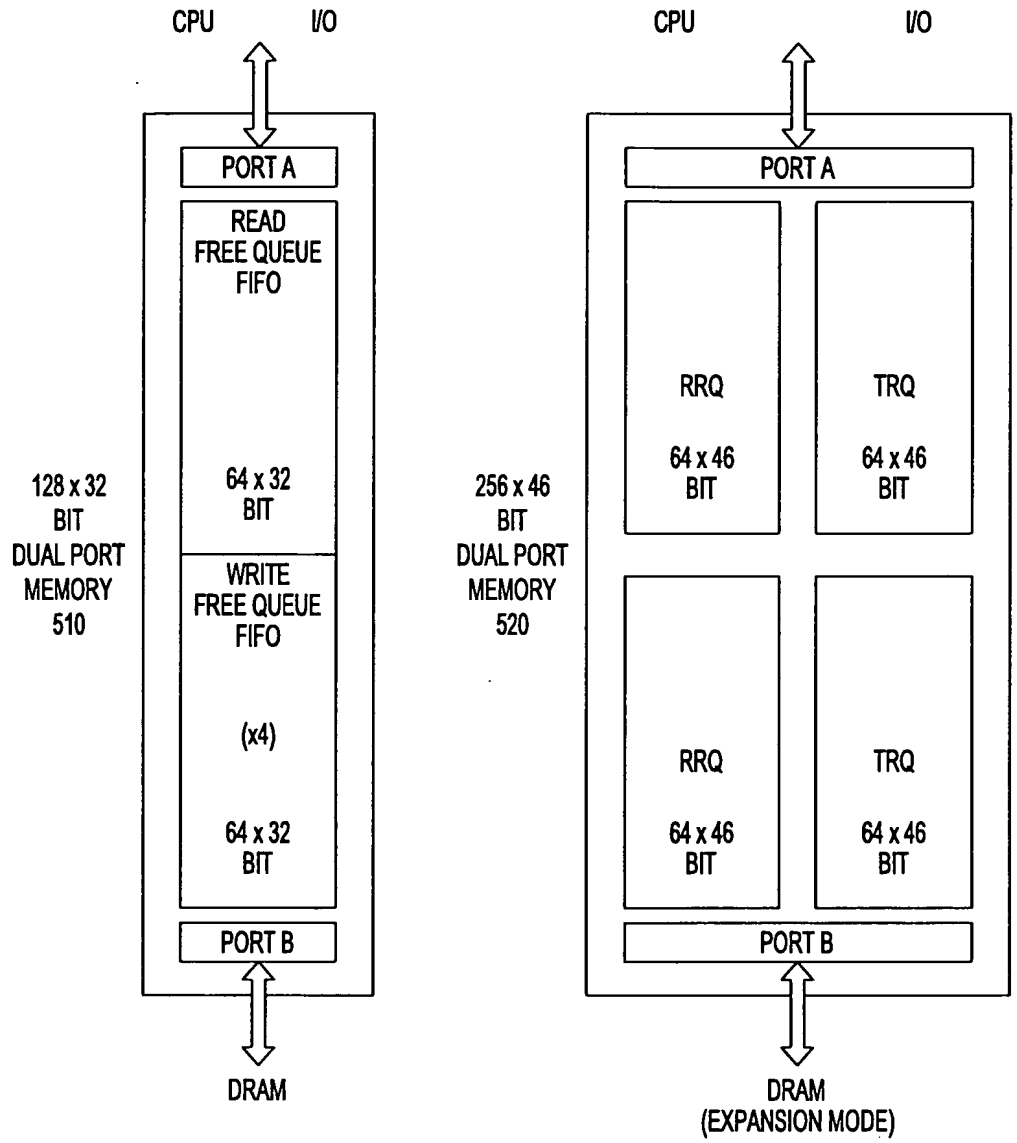

CPU
I/O
PORT A
READ FREE QUEUE FIFO
64 x 32 BIT
WRITE FREE QUEUE FIFO
(x4)
64 x 32 BIT
PORT B
128 x 32 BIT DUAL PORT MEMORY 510
DRAM
CPU
I/O
PORT A
RRQ
64 x 46 BIT
TRQ
64 x 46 BIT
RRQ
64 x 46 BIT
TRQ
64 x 46 BIT
PORT B
256 x 46 BIT DUAL PORT MEMORY 520
DRAM (EXPANSION MODE)

FIG. 5

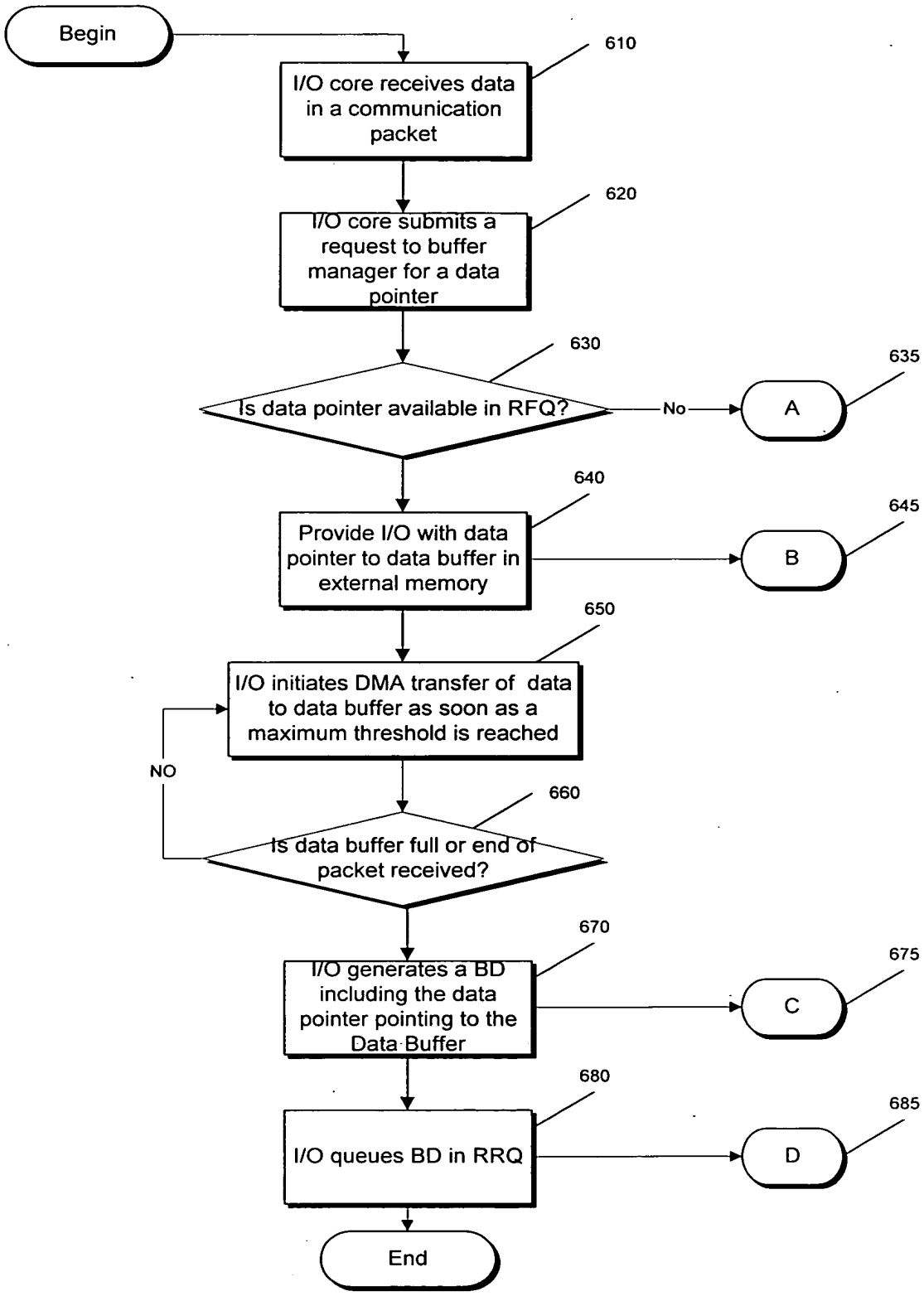

Begin
610
I/O core receives data in a communication packet
620
I/O core submits a request to buffer manager for a data pointer
630
Is data pointer available in RFQ?
No
635
A
640
Provide I/O with data pointer to data buffer in external memory
645
B
650
I/O initiates DMA transfer of data to data buffer as soon as a maximum threshold is reached
NO
660
Is data buffer full or end of packet received?
670
I/O generates a BD including the data pointer pointing to the Data Buffer
675
C
680
I/O queues BD in RRQ
685
D
End

FIG.6

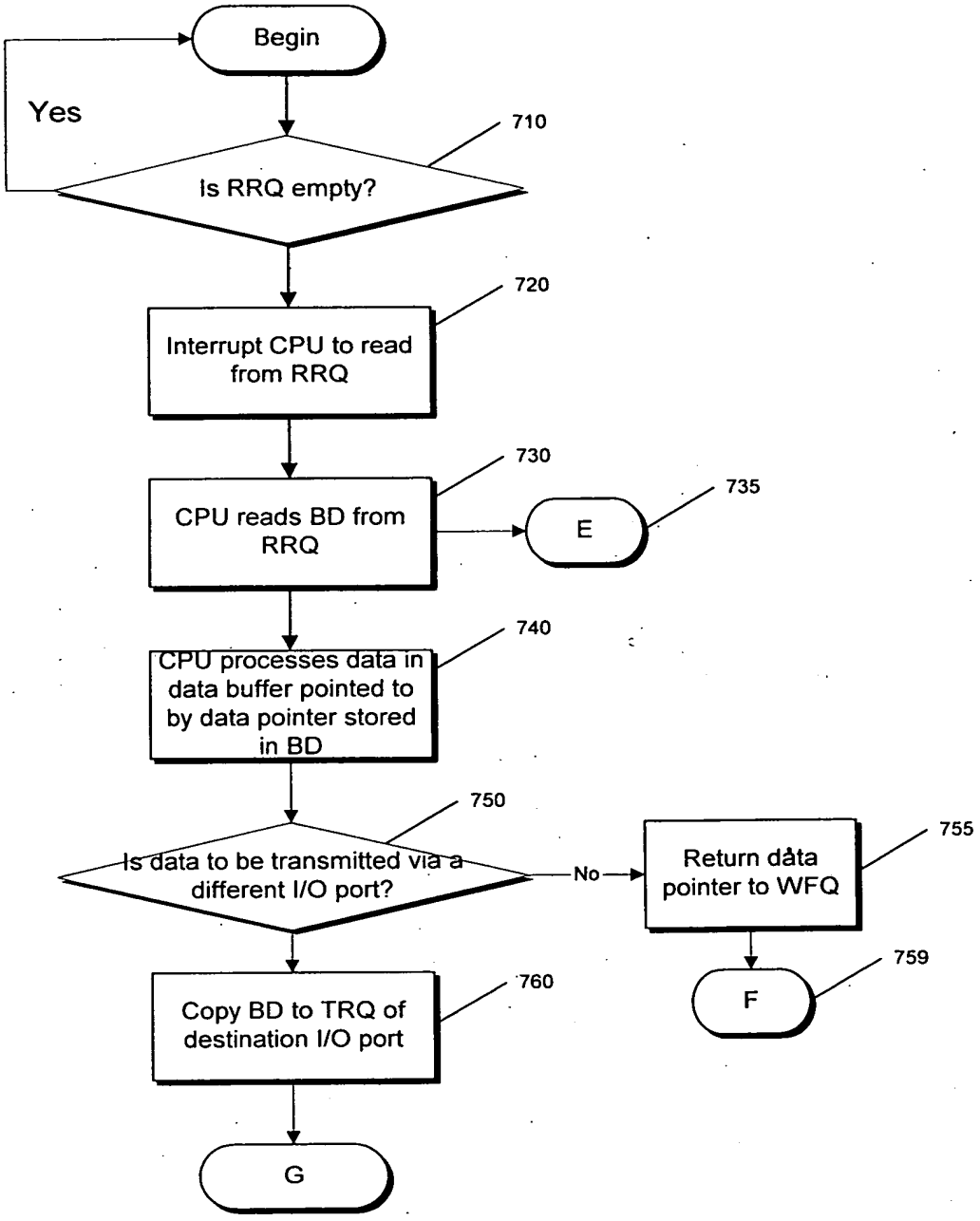

Begin
Yes
710
Is RRQ empty?
720
Interrupt CPU to read from RRQ
730
CPU reads BD from RRQ
E
735
740
CPU processes data in data buffer pointed to by data pointer stored in BD
750
Is data to be transmitted via a different I/O port?
No
Return data pointer to WFQ
755
F
759
Copy BD to TRQ of destination I/O port
760
G

FIG. 7

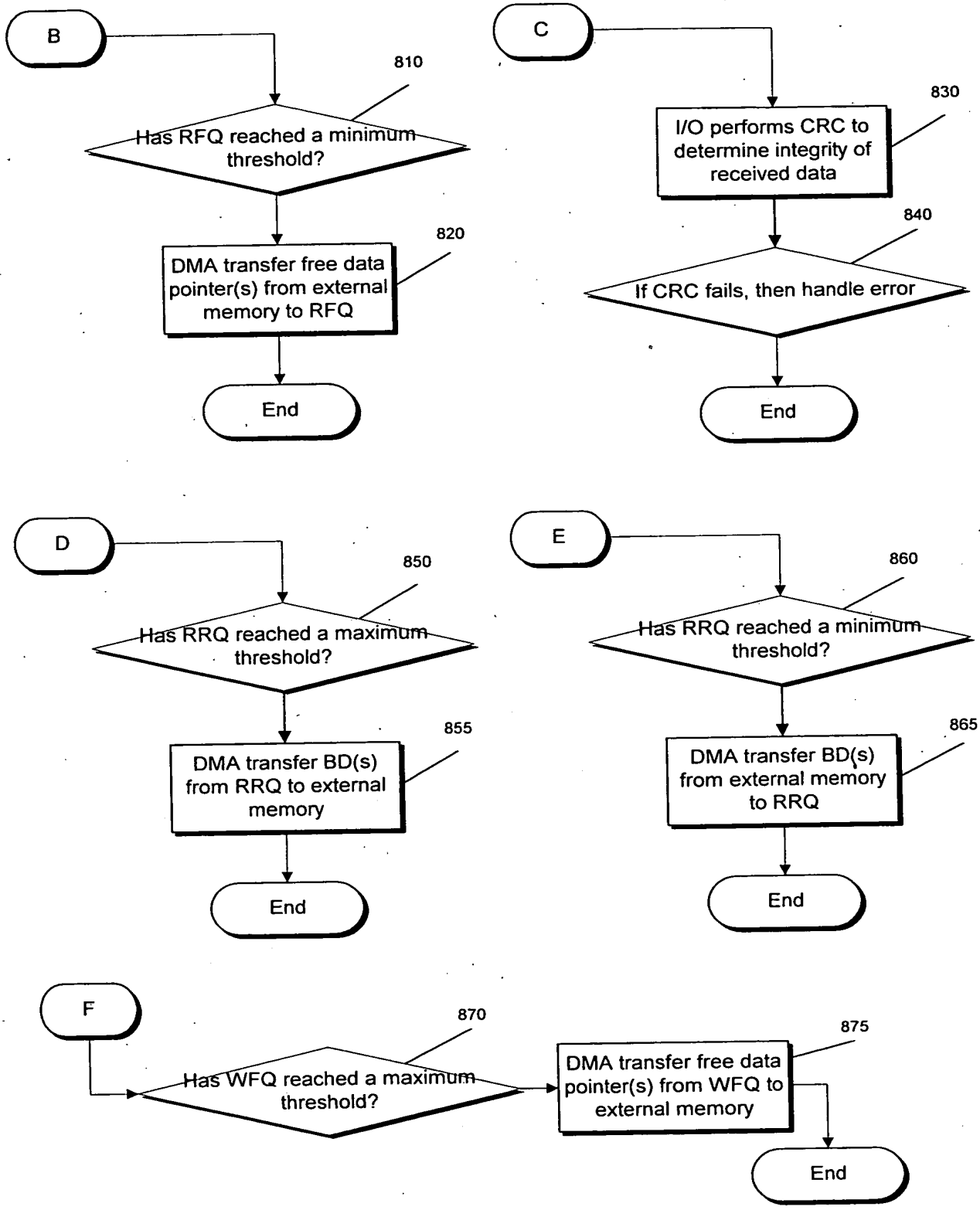

B
810
Has RFQ reached a minimum threshold?
820
DMA transfer free data pointer(s) from external memory to RFQ
End
C
830
I/O performs CRC to determine integrity of received data
840
If CRC fails, then handle error
End
D
850
Has RRQ reached a maximum threshold?
855
DMA transfer BD(s) from RRQ to external memory
End
E
860
Has RRQ reached a minimum threshold?
865
DMA transfer BD(s) from external memory to RRQ
End
F
870
Has WFQ reached a maximum threshold?
875
DMA transfer free data pointer(s) from WFQ to external memory
End

FIG.8

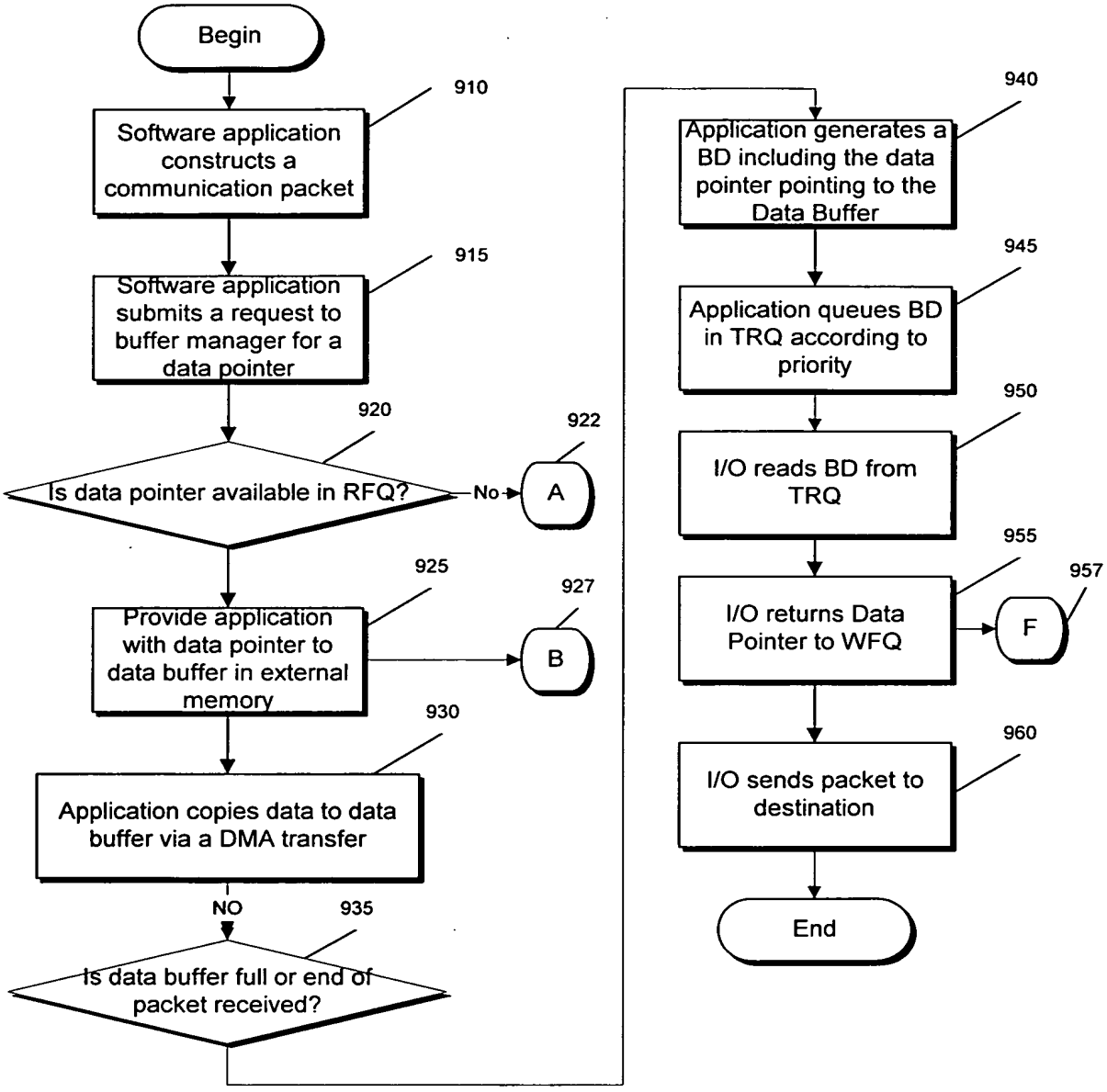

Begin
910
Software application constructs a communication packet
915
Software application submits a request to buffer manager for a data pointer
920
Is data pointer available in RFQ?
No
922
A
925
Provide application with data pointer to data buffer in external memory
927
B
930
Application copies data to data buffer via a DMA transfer
NO
935
Is data buffer full or end of packet received?
940
Application generates a BD including the data pointer pointing to the Data Buffer
945
Application queues BD in TRQ according to priority
950
I/O reads BD from TRQ
955
I/O returns Data Pointer to WFQ
957
F
960
I/O sends packet to destination
End

FIG.9

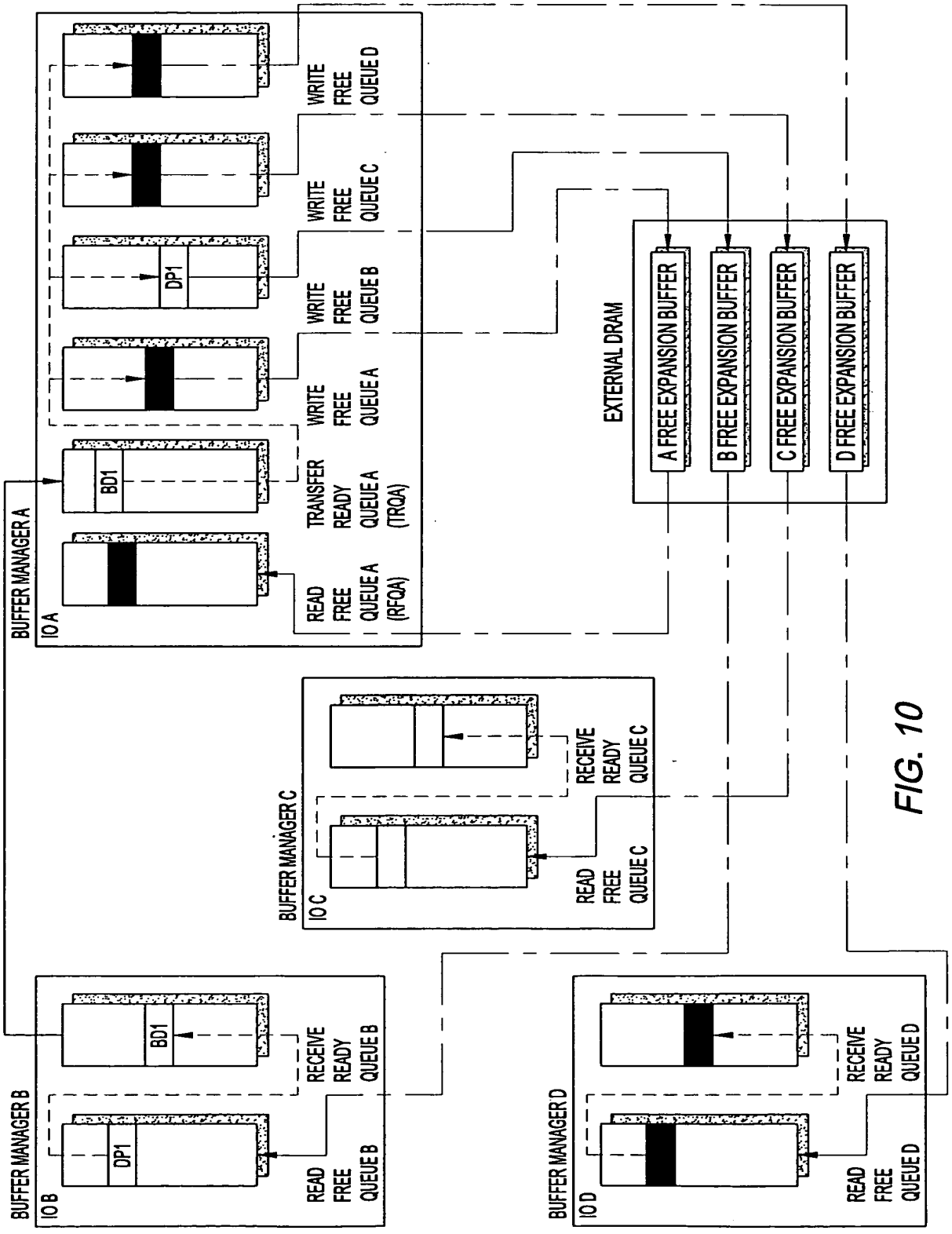

BUFFER MANAGER A
IO A
READ FREE QUEUE A (RFQA)
TRANSFER READY QUEUE A (TRQA)
WRITE FREE QUEUE A
WRITE FREE QUEUE B
WRITE FREE QUEUE C
WRITE FREE QUEUE D
BD1
DP1
EXTERNAL DRAM
A FREE EXPANSION BUFFER
B FREE EXPANSION BUFFER
C FREE EXPANSION BUFFER
D FREE EXPANSION BUFFER
BUFFER MANAGER C
IO C
READ FREE QUEUE C
RECEIVE READY QUEUE C
BUFFER MANAGER B
IO B
READ FREE QUEUE B
RECEIVE READY QUEUE B
BUFFER MANAGER D
IO D
READ FREE QUEUE D
RECEIVE READY QUEUE D

FIG. 10

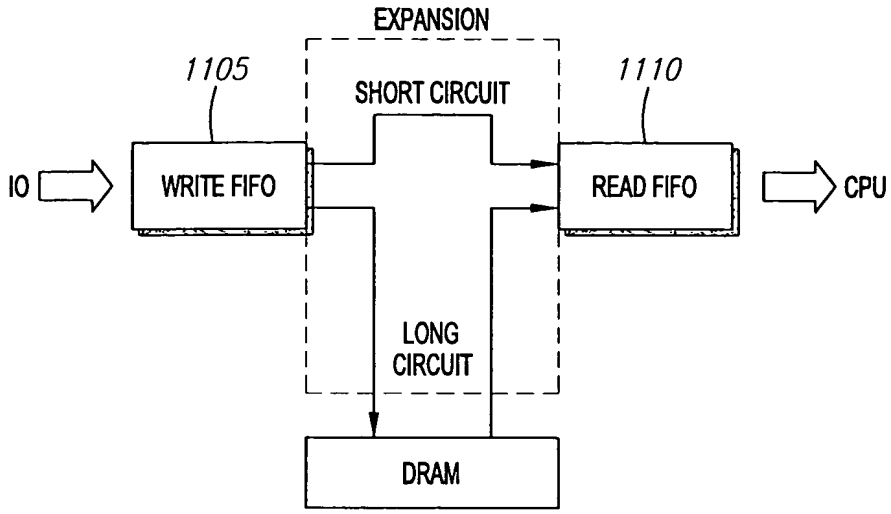

EXPANSION
1105
SHORT CIRCUIT
1110
IO
WRITE FIFO
READ FIFO
CPU
LONG CIRCUIT
DRAM

FIG. 11

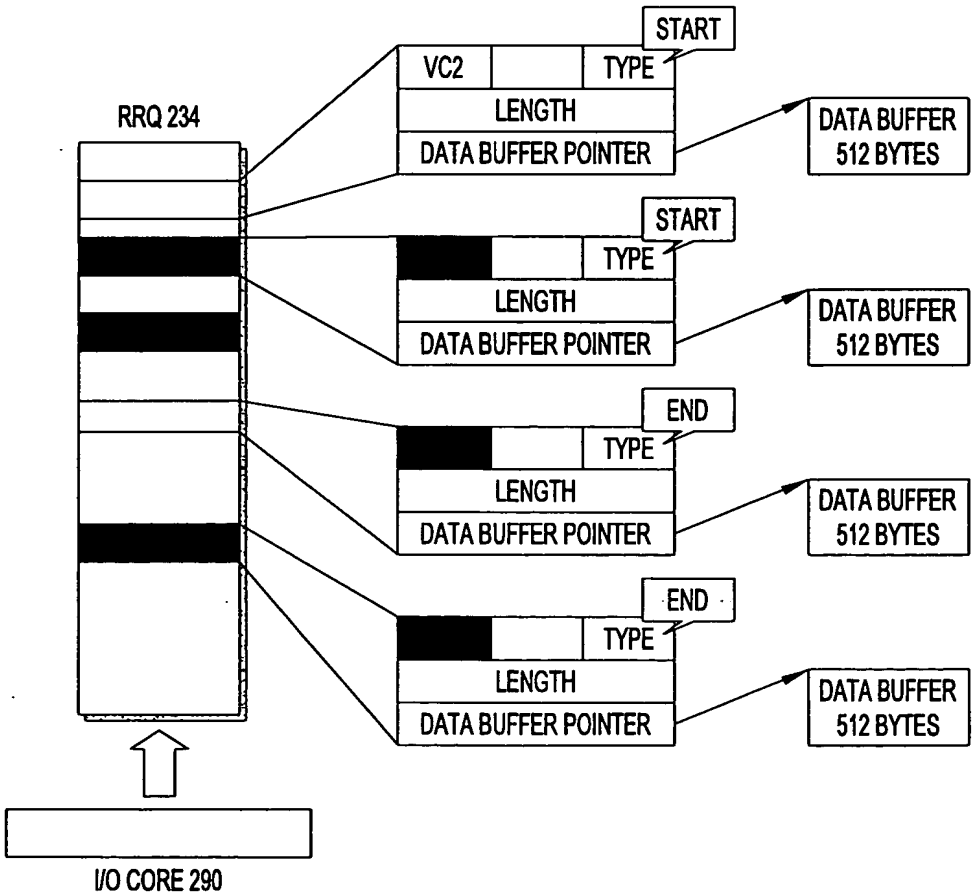

RRQ 234
START
VC2
TYPE
LENGTH
DATA BUFFER POINTER
DATA BUFFER 512 BYTES
START
TYPE
LENGTH
DATA BUFFER POINTER
DATA BUFFER 512 BYTES
END
TYPE
LENGTH
DATA BUFFER POINTER
DATA BUFFER 512 BYTES
END
TYPE
LENGTH
DATA BUFFER POINTER
DATA BUFFER 512 BYTES
I/O CORE 290

FIG. 12

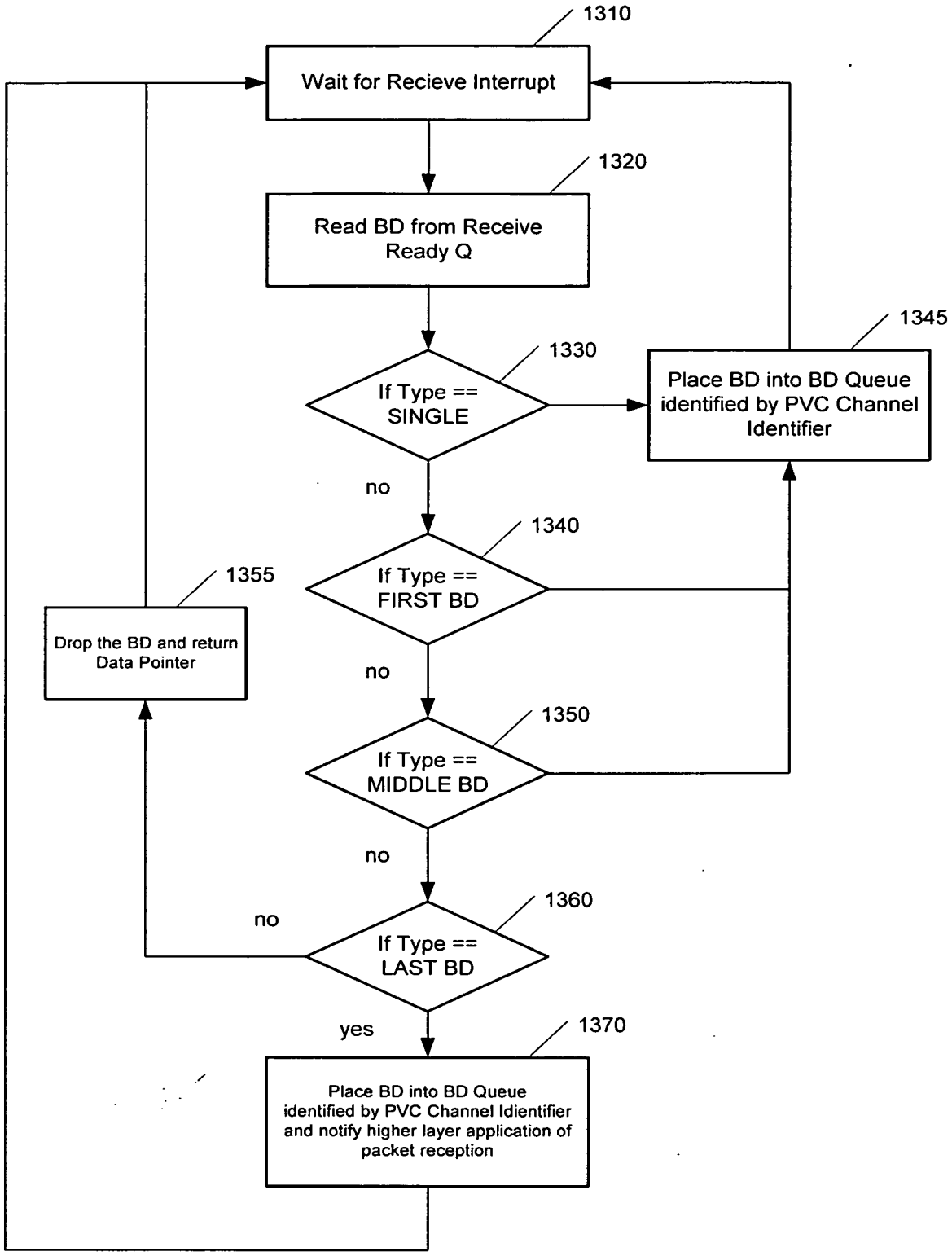

1310
Wait for Recieve Interrupt
1320
Read BD from Receive Ready Q
1330
If Type == SINGLE
1345
Place BD into BD Queue identified by PVC Channel Identifier
no
1340
If Type == FIRST BD
1355
Drop the BD and return Data Pointer
no
1350
If Type == MIDDLE BD
no
1360
If Type == LAST BD
no
yes
1370
Place BD into BD Queue identified by PVC Channel Idientifier and notify higher layer application of packet reception

FIG. 13

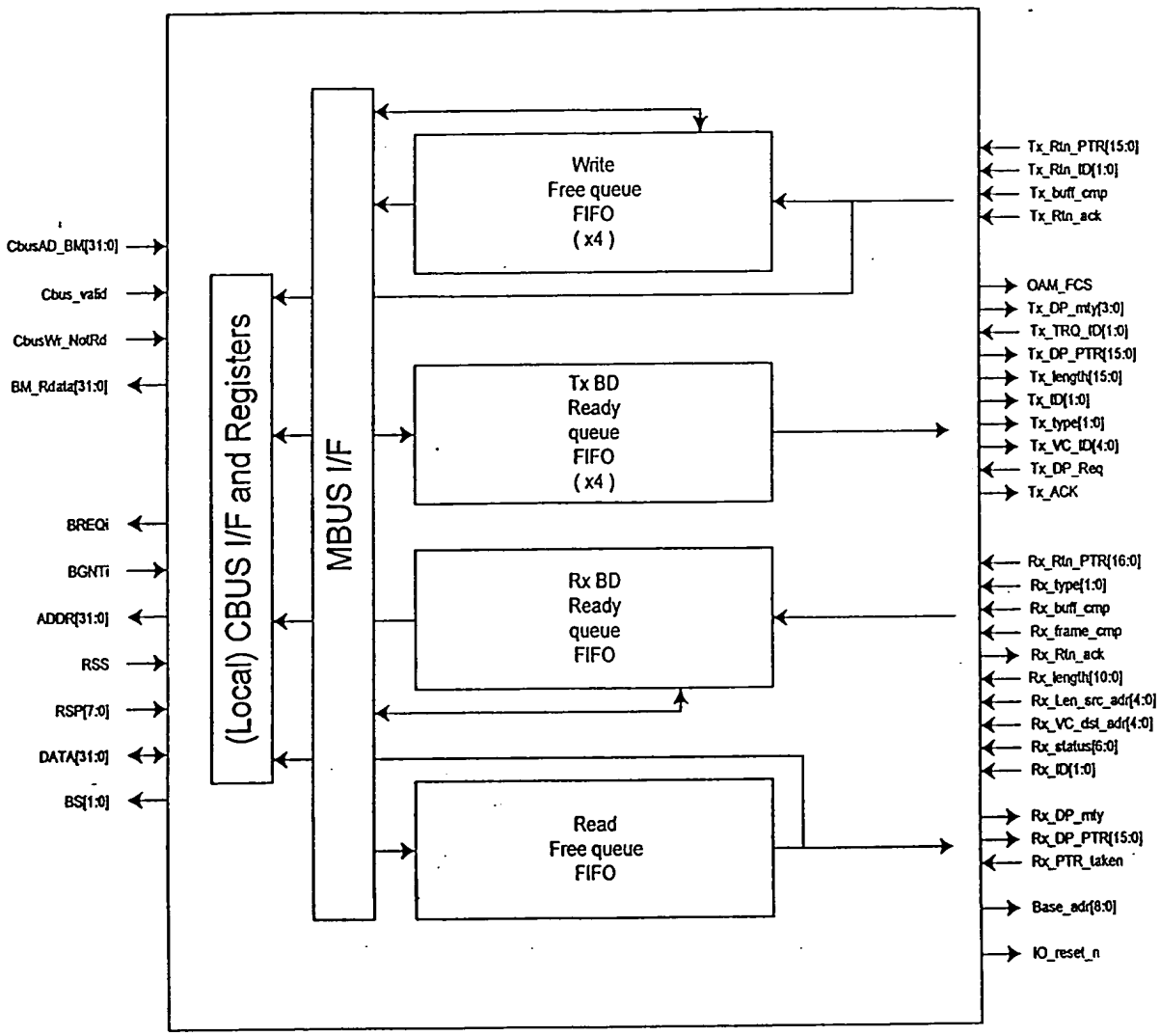

CbusAD_BM[31:0]
Cbus_valid
CbusWr_NotRd
BM_Rdata[31:0]
BREQi
BGNTi
ADDR[31:0]
RSS
RSP[7:0]
DATA[31:0]
BS[1:0]
(Local) CBUS I/F and Registers
MBUS I/F
Write Free queue FIFO (x4)
Tx BD Ready queue FIFO (x4)
Rx BD Ready queue FIFO
Read Free queue FIFO
Tx_Rtn_PTR[15:0]
Tx_Rtn_ID[1:0]
Tx_buff_cmp
Tx_Rtn_ack
OAM_FCS
Tx_DP_mty[3:0]
Tx_TRQ_ID[1:0]
Tx_DP_PTR[15:0]
Tx_length[15:0]
Tx_ID[1:0]
Tx_type[1:0]
Tx_VC_ID[4:0]
Tx_DP_Req
Tx_ACK
Rx_Rtn_PTR[16:0]
Rx_type[1:0]
Rx_buff_cmp
Rx_frame_cmp
Rx_Rtn_ack
Rx_length[10:0]
Rx_Len_src_adr[4:0]
Rx_VC_dst_adr[4:0]
Rx_status[6:0]
Rx_ID[1:0]
Rx_DP_mty
Rx_DP_PTR[15:0]
Rx_PTR_taken
Base_adr[8:0]
IO_reset_n

FIG. 14